

### General Description

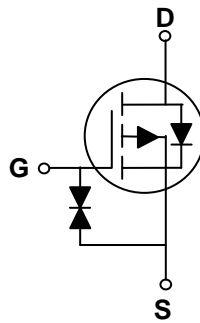
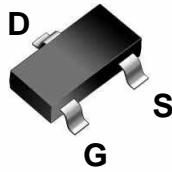
These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

### Features

$V_{DS}$	-20V
$I_D$ (at $V_{GS}=-4.5V$ )	-0.5A
$R_{DS(ON)}$ (at $V_{GS}=-4.5V$ )	580mΩ(Typ)

ESD Protected Up to 2.0KV (HBM)

SOT723



### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units	
Drain-Source Voltage	$V_{DS}$	-20	V	
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V	
Drain Current-Continuous	TC=25°C	$I_D$	-0.5	A
	TC=100°C	$I_D$	-0.4	A
Maximum Power Dissipation	$P_D$	0.18	W	
Drain Current – Pulsed1	$I_{DM}$	-2.6	A	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	°C	

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance junction-to-solder point	$R_{\theta JSP}$		40	°C /W
Thermal Resistance junction-to-Ambient	$R_{\theta JA}$		500	°C /W

## Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-20			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V			1	μA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> =±10V, V <sub>DS</sub> =0V			±10	μA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-0.3	-0.6	-1.2	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-0.5A		580	850	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-0.3A		850	1200	mΩ
		V <sub>GS</sub> =-1.8V, I <sub>D</sub> =-0.2A		1350	2000	mΩ
I <sub>S</sub>	Maximum Body-Diode Continuous Current				-0.5	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-10V, V <sub>GS</sub> =0V, F=1.0MHz		71		pF
C <sub>OSS</sub>	Output Capacitance			20		pF
C <sub>rSS</sub>	Reverse Transfer Capacitance			15		pF
<b>SWITCHING PARAMETERS</b>						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> =-10V, I <sub>D</sub> =-0.2A, V <sub>GS</sub> =-4.5V, R <sub>G</sub> =10Ω		4		nS
t <sub>r</sub>	Turn-on Rise Time			19		nS
t <sub>d(off)</sub>	Turn-Off Delay Time			16		nS
t <sub>f</sub>	Turn-Off Fall Time			25		nS
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =-10V, I <sub>D</sub> =-0.2A, V <sub>GS</sub> =-4.5V		1.2		nC
Q <sub>gs</sub>	Gate-Source Charge			0.37		nC
Q <sub>gd</sub>	Gate-Drain Charge			0.27		nC
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>SD</sub> =-1A		0.7	1.2	V

Note:

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
3. Essentially independent of operating temperature.

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

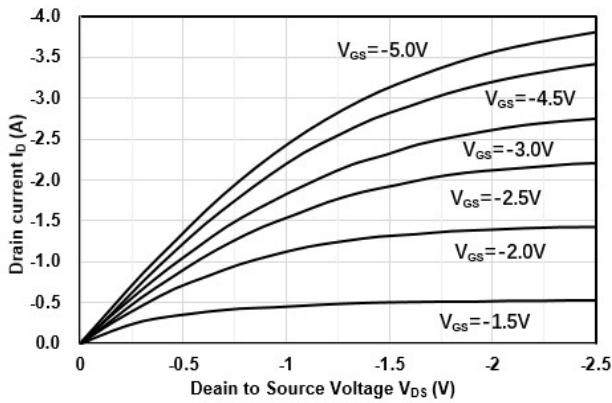


Figure1. Output Characteristics

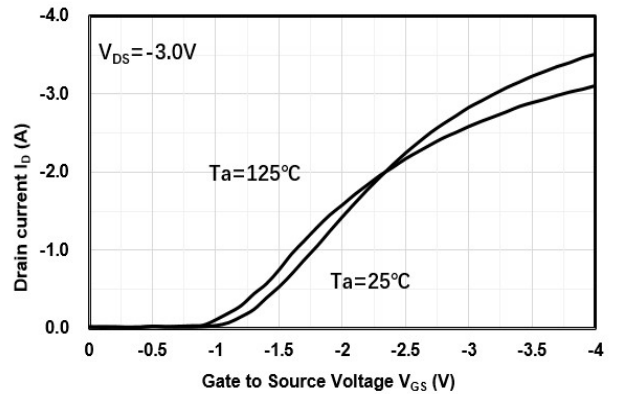


Figure2. Transfer Characteristics

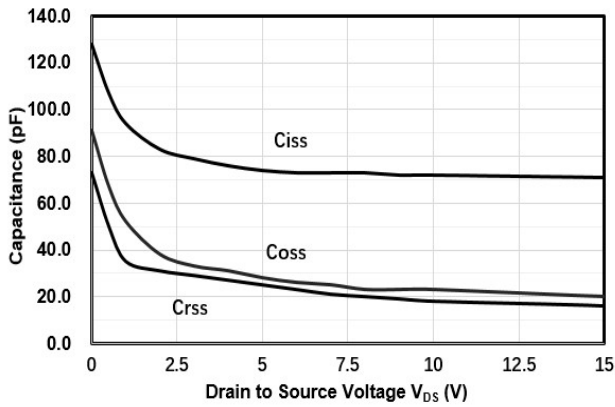


Figure3. Capacitance Characteristics

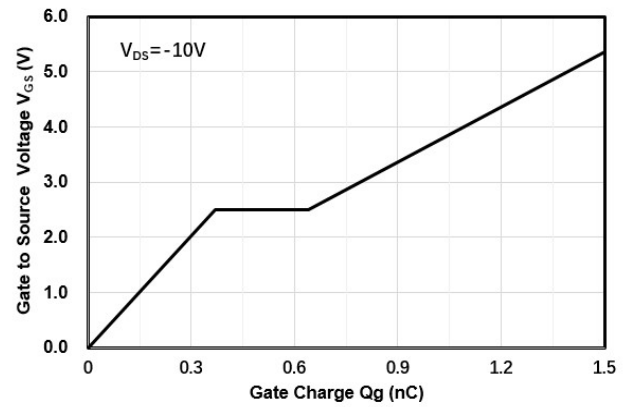


Figure4. Gate Charge

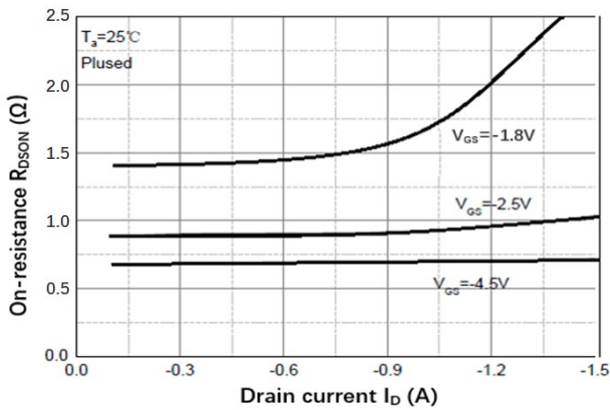


Figure5. Drain-Source on Resistance

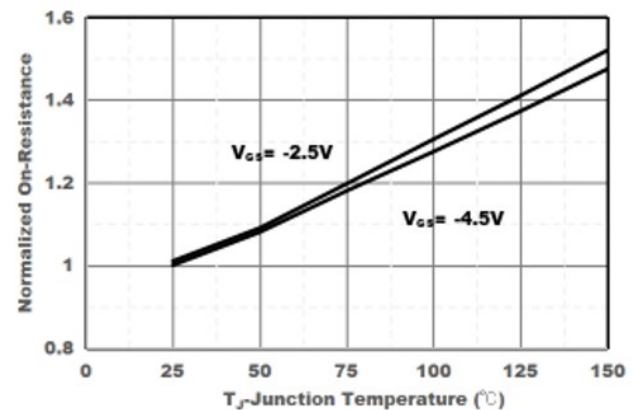


Figure6. Drain-Source on Resistance

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

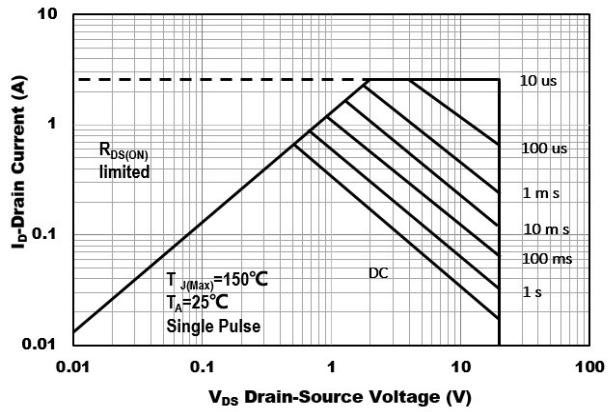


Figure7. Safe Operation Area

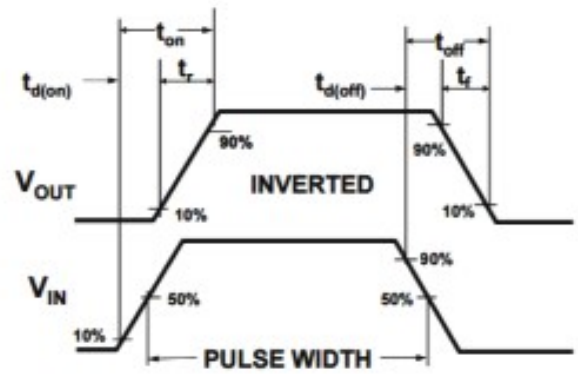
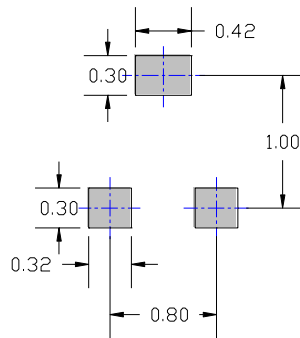
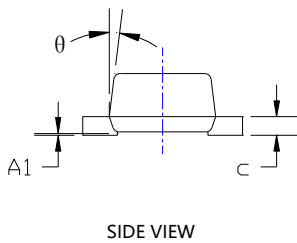
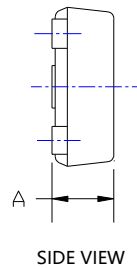
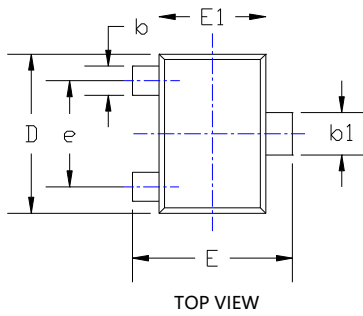


Figure8. Switching wave

**SOT723 PACKAGE INFORMATION**



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.017	0.022	0.430	0.550
A1	0.000	0.002	0.000	0.050
b	0.007	0.011	0.170	0.270
b1	0.011	0.015	0.270	0.370
c	0.003	0.008	0.080	0.200
D	0.045	0.049	1.150	1.250
E	0.045	0.049	1.150	1.250
E1	0.030	0.033	0.750	0.850
e	0.031TYP.		0.800TYP.	
θ	7°REF.		7°REF.	

NOTE:  
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.  
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.  
 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.