杭芯科技
HUTCHIP

HCNR05P20

-200V P-Channel MOSFET

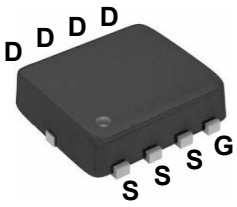
General Description

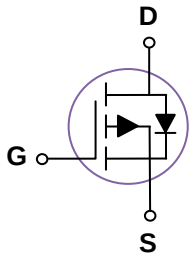
These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features

V_{DS}	-200V
I_D (at V_{GS}=-10V)	-5A
$R_{DS(ON)}$ (at V_{GS}=-10V)	1.4Ω(Typ)

PDFN3*3





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-200	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuous	TC=25°C	I_D	-5	A
	TC=100°C	I_D	-4	A
Maximum Power Dissipation		P_D	35	W
Drain Current – Pulsed1		I_{DM}	-20	A
Single pulse avalanche energy[a5]		E_{AS}	-20	mJ
Junction and Storage Temperature Range		T_J,T_{STG}	-55 To 150	℃

Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance junction-case	$R_{\theta Jc}$		3.57	℃ /W
Thermal Resistance junction-to-Ambient	$R_{\theta JA}$		62	℃ /W

Electrical Characteristics (TJ=25℃ unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=-250μA	-200			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-200V,V_{GS}=0V			1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=-±20,V_{DS}=0V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=-250μA	-2.5	-3.5	-4.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=-10V, I_D=-2.5A		1.4	1.7	Ω
DYNAMIC PARAMETERS						
Ciss	Input Capacitance	V_{DS}=-25V,V_{GS}=0V, F=1.0MHz		480		pF
C_{oss}	Output Capacitance			100		pF
C_{rss}	Reverse Transfer Capacitance			30		pF
SWITCHING PARAMETERS						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=-160V,I_D=-2.5A V_{GS}=-10V R_G=9.1Ω		15		nS
t_r	Turn-on Rise Time			25		nS
$t_{d(off)}$	Turn-Off Delay Time			20		nS
t_f	Turn-Off Fall Time			15		nS
Q_g	Total Gate Charge	V_{DS}=-160V,I_D=-5A, V_{GS}=-10V		18		nC
Q_{gs}	Gate-Source Charge			9		nC
Q_{gd}	Gate-Drain Charge			8		nC
V_{SD}	Diode Forward Voltage	V_{GS}=0V,I_{SD}=-3A			1.2	V

Note：

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
3. Essentially independent of operating temperature.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

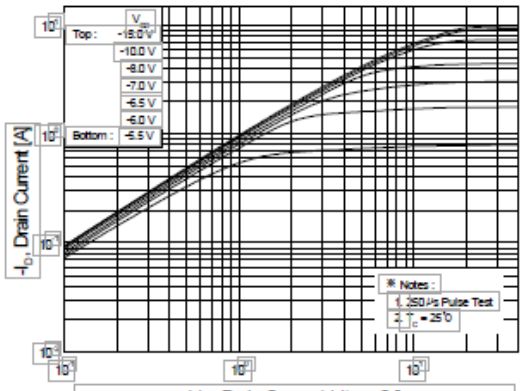


Figure 1. On-Region Characteristics

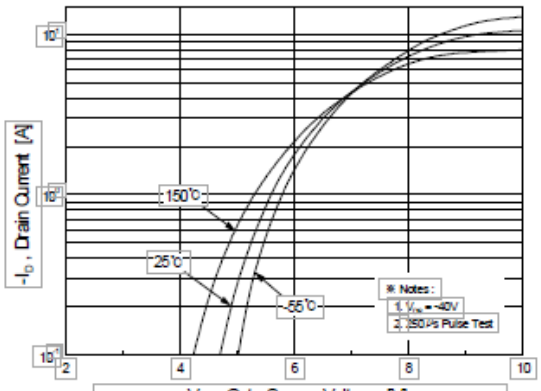


Figure 2. Transfer Characteristics

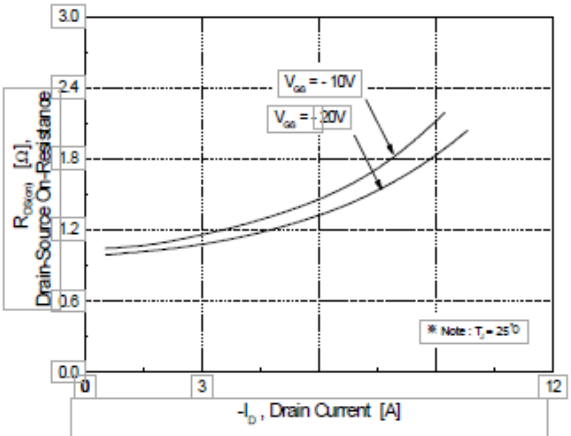


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

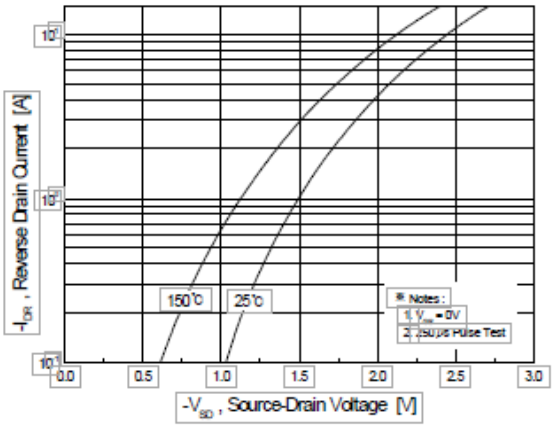


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

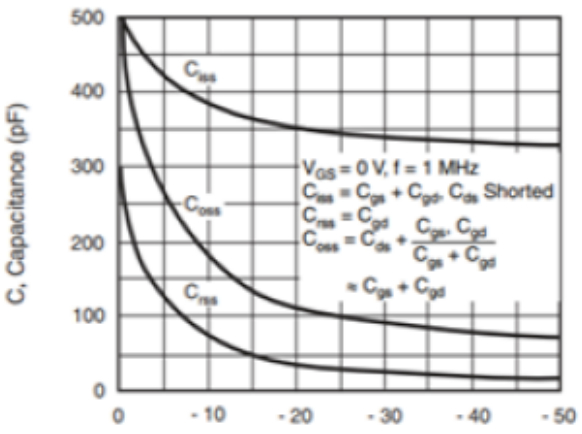


Figure 5. Capacitance Characteristics

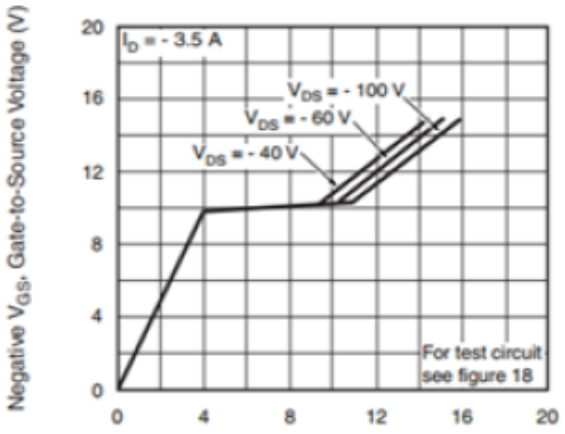


Figure 6. Gate Charge Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

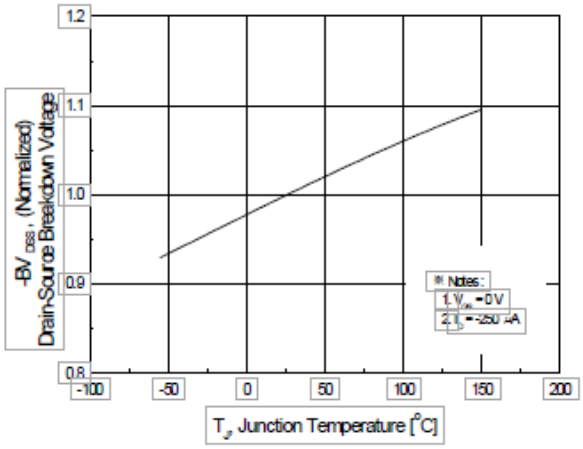


Figure 7. Breakdown Voltage Variation vs. Temperature

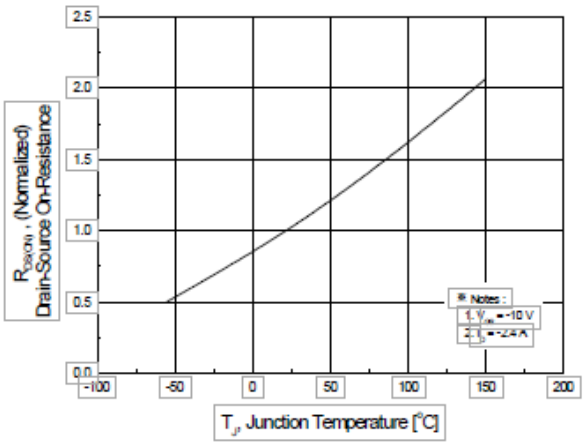


Figure 8. On-Resistance Variation vs. Temperature

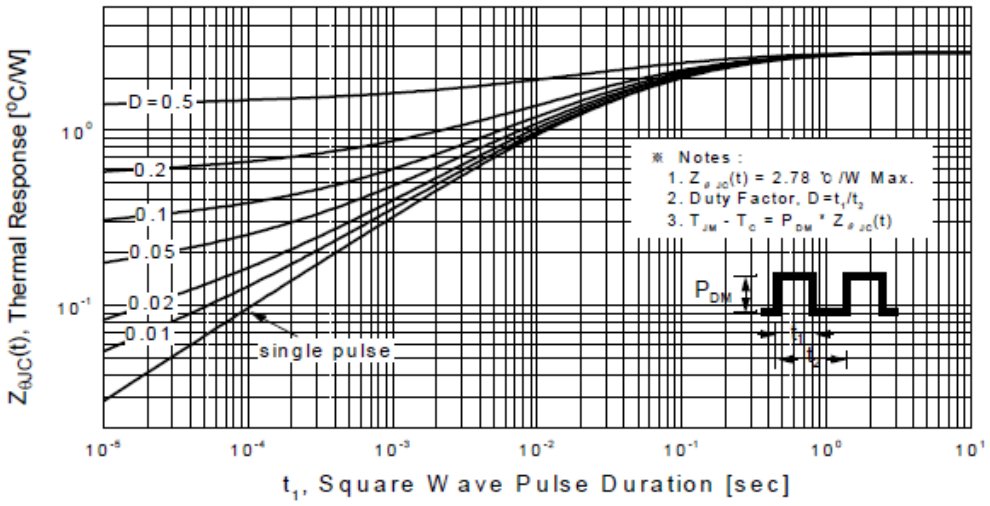
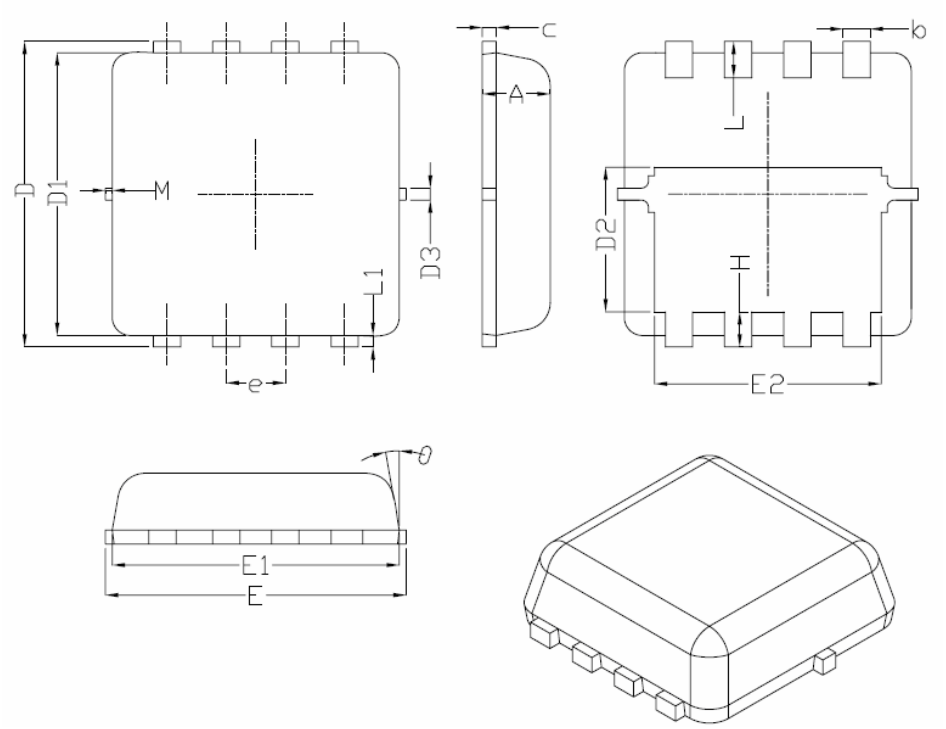


Figure 9. Normalized Maximum Transient Thermal Impedance

PDFN3x3 PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.48	1.58	1.68
D3	-	0.13	-
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BS		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	-	0.13	-
M	*	*	0.15
θ		10°	12°